REMARKS

Claims 1, 3-4 and 8-10 are pending in this application, of which claims 1, 3-4 have been amended and claims 8-10 are newly-added. Claims 2 and 5-7 have been canceled.

The Examiner has objected to claim 1 for various informalities which have been corrected in the aforementioned amendments.

Claim 1 stands rejected under 35 U.S.C. §102(b) as anticipated by Onizuka et al., The Fundamentals and Frontiers 2003 Conference of Nen The Institute of Electronics, Information and Communications Engineers Kiso Kyokai Society Taikai Koen Ronbunshu; Japan, 09/18/2003, (hereinafter "**Onizuka et al.**").

Applicants respectfully traverse this rejection.

Onizuka et al., which is in Japanese, shows chip 1 and chip 2 arranged side-by-side schematically, where each chip contains a circuit containing a coil ("L_1" in chip 1 and "L_2" in chip 2) and the coils are arranged in close proximity to each other.

Onizuka et al., discloses power transmission between two chips by inductive coupling, but fails to disclose signal transmission in the manner recited in claim 1, as amended.

Accordingly, the 35 U.S.C. §102(b) rejection should be withdrawn.

Claims 2-7 stand rejected under 35 U.S.C. §103(a) as unpatentable over **Onizuka et al.** in view of U.S. Patent 5,701,037 to Weber et al. (hereinafter **Weber et al.**).

Applicants respectfully traverse this rejection.

Weber et al. discloses an arrangement for signal transmission between chip layers of a vertically integrated circuit, such that "a defined, inductive signal transmission ensues between a part of the vertically integrated circuit in one chip layer and a further part of the vertically integrated circuit in a further chip layer by means of a

coupling inductance formed by respective coils in the two layers. Particularly given high connection densities, a large number of freely placeable and reliable vertical signal connections can be produced directly from the inside of one chip layer to the inside of a neighboring chip layer without extremely high demands being made on the adjustment of the chip layers relative to one another and on the surface planarity of the individual chip layers." (see "Abstract")

Weber et al. has been cited for teaching the transmitter circuit of claim 2 and the receiver circuit of claim 3, among other things.

Applicants admit that **Weber et al.** discloses "Signal transmission between two chip layers by inductive coupling" (see Fig. 1), but **Weber et al.** fails to disclose that a first receiver circuit in a second substrate and a second receiver circuit in a third substrate receive a digital signal transmitted by a transmitter circuit in a first substrate by inductive coupling, as in the present invention.

The Examiner commented that "**Weber et al.** teaches the coils L2 on each of the plurality of the stacked chip layers (col. 3; 18-19)" (page 5, 8-7th lines from the bottom). **Weber et al.** teaches a plurality of chips, but **Weber et al.** fails to teach a plurality of coils L2 (see Fig. 1), as recited in claim 1, as amended, from which claims 3 and 4 depend.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1, 3-4 and 8-10, as amended, are in condition for allowance, which action, at an early date, is requested.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1105.

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Respectfully submitted,

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